REMARKS

Upon entry of this Response, claims 1-27 remain pending in the present patent application. While no amendments are offered herein, the claims are listed as originally filed for the sake of convenience. Applicants request the reconsideration of pending claims in view of the following remarks.

In item 2 of the Office Action, claims 1, 11-12, 13, 18-19, 20, and 25-27 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,472,899 issued to Osburn et al. (hereafter "*Osburn*"). Anticipation under §102 "requires the disclosure in a single prior are reference of each element of the claim under construction. W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983). For the reasons that follow, Applicants respectfully requests the rejection of these claims be withdrawn.

To begin, claim 1 states as follows:

> 1. A method, comprising:
> determining a worst-case impedance of a power supply loop coupled to a power input of a die;
> determining a reference voltage at the power input of the die associated with an average current generated at a power supply included in the power supply loop;
> measuring a maximum change in a current at the power input of the die; and
> calculating an estimate of a worst-case voltage at the power input of the die based upon the worst-case impedance, the reference voltage, and the maximum change in the current.

With respect to claim 1, the Office Action states:

"As per Claim 1, Osburn discloses a method, comprising:

- determining a worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages) of a power supply loop coupled to a power input (Power Supply, Indicated as PS in FIG. 1) of a die (Integrated circuit, IC 102);
- determining a reference voltage (block 202 in FIG. 2) at the power input of the die associated with an average current generated at a power supply included in the power supply loop;
- measuring a maximum change in a current (column 5, lines 22-28, see FIG. 3) at the power input of the die; and
- measuring a maximum change in a current (column 5, lines 22-28, see FIG. 3) at the power input of the die; and calculating an estimate of a worst-case voltage (column 4, lines 1-5) at the power input of the die based up-on the worst-case impedance, the reference voltage, and the maximum change in the current." (Office Action, pgs. 2-3.)

As set forth in claim 1, the worst-case impedance is determined of a power supply loop coupled to a power input of a die. The Office Action points to the minimum and maximum load lines slopes of FIG. 3 of *Osburn* as showing or suggesting the worst-case impedance of a power supply loop coupled to the power input of a die.

Applicants respectfully disagree as the load line slopes are generated based on the data printed about the integrated circuits as set forth by a manufacturer, and are not worst-case impedance as determined of a power supply loop that is coupled to a power input of a die. In this respect, the worst-case impedance measured of an actual power supply loop may vary from values provided from a manufacturer on literature. In addition, measuring the worst-impedance is difficult as the tools employed to measure the various characteristics of the power supply loop change the electrical properties of the loop when applied. The values discussed by *Osburn* do not take such complexities into account.

Also, claim 1 as originally filed provides for determining a reference voltage at the power input of the die associated with an average current generated at a power supply included in the power supply loop. The "reference voltage" referred to by *Osburn* refers to a "voltage identification" (VID) of an integrated circuit product. Specifically, the reference voltage referred to by *Osburn* is merely a voltage setting associated with an integrated circuit, and is not determined at the power input of the die with an average current generated at the power supply as set forth in claim 1.

Also, *Osburn* fails to show or suggest the measuring of a maximum change in a current at the power input of the die. Specifically, *Osburn* fails to show or suggest any measuring of the change in current at all. With respect to this element, the Office Action cites column 5, lines 22-28 and FIG. 3 of *Osburn*. However, at column 5, lines 12-27 inclusive of this cited section, *Osburn* states:

> "Now the process **200** calculates the load line slope (block **214**). For example, the transient minimum load line slope can be calculated since the maximum transient minimum load line data point **312** and the minimum transient minimum load line data point **304** are known. FIG. 3 shows the transient minimum load line **320** and its associated slope. Using the calculated transient minimum load line slope, other load lines, having the same or similar slope, can then be calculated. Not all load lines maintain the same slope or linearity. Some load lines may have different slopes or event be somewhat non-linear to account for variations due to current I_{CC} effects that change with I_{CC} magnitude (e.g., the

> transient minimum 320 and maximum 328 load lines flair out at the high current and low current levels respectively to account for load I_{CC} change variations and their affects on voltage transients)." (Office Action, col. 5, lines 13-28.)

Nowhere does *Osbum* show or suggest that the maximum change in current at the power input of the die is measured as set forth in claim 1. Rather, the values are merely calculated based on manufacturer provided values as described above.

In addition, the Office Action states that *Osbum* calculates an estimated worst-case voltage at the power input of the die based upon the worst-case impedance, the reference voltage, and the maximum change in current. In support of this contention, the Office Action cites column 4, lines 1-5 of *Osbum*. However, at column 3, line 60 - column 4, line 8, inclusive of the above-cited portion, *Osbum* states:

> "Next, at block **208**, the process **200** defines the minimum voltage allowed at the maximum current draw I_{CC}. As shown in FIG. **3**, a minimum transient minimum load data point **304**, at the maximum current draw I_{CC} (e.g. 30 amps), is defined to be offset approximately - 160 mV from the VID setting, or at approximately 1.44 V. Because the critical factor in stable operation of an IC product is the minimum voltage level at any given operational state, the primary goal for stable operation is to ensure that input voltage levels are above the minimum level under worst-case conditions. Thus, if the voltage is required to droop with increasing current levels, then the worst-case voltage V_{CC} occurs at the worst case current draw I_{CC} for a given IC product. In this example, this occurs at approximately - 160 mV, with a current draw of 30 amps, at the minimum transient minimum load data point **304**." (Office Action, col. 3, lines 60-67 and col. 4, lines 1-8.)

The above excerpt does not show or suggest calculating a worst-case voltage based upon the worst-case impedance, the reference voltage, and the maximum change in current. In fact, the concept of the worst-case impedance is not even discussed. The values employed are those provided on paper, rather than measured values as set forth in claim 1. Similarly, since the reference voltage is not obtained as described above in claim 1 as set forth above, it cannot be that an estimate of the worst-case voltage is based upon such information as claimed.

Accordingly, for the above reasons, Applicants assert that the rejection of claim 1 is improper. In addition, Applicants assert that the rejection of claims 13, 20, and 27 are improper for at least the reasons described above with reference to claim 1 to the extent such reasons apply. Accordingly, Applicants request that the

rejection of claims 1, 13, 20, and 27 be withdrawn. In addition, Applicants request that the rejection of claims 11, 12, 18, 19, 25, and 26 be withdrawn as depending from claims 1, 13, or 20, respectively.

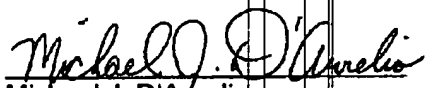
In addition, claim 10 has been rejected under 35 U.S.C. §103(a) as being unpatentable over *Osburn* in view of U.S. Patent 5,949,798 issued to Sakaguchi (hereafter "*Sakaguchi*"). A prima facie case of obviousness is established only when the prior art teaches or suggests all of the elements of the claims. MPEP §2143.03, In re Riickaert, 9 F.3d 1531, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). Applicants assert that the cited combination of references falls to show or suggest each of the elements of claim 10 as depending from claim 1 above for the reasons described above with respect to claim 1. Accordingly, Applicants request that the rejection of claim 10 be withdrawn.

In addition, in Item 5 of the Office Action, claims 2-9, 14-17 and 21-24 have been objected to as being dependant upon a rejected base claim, but would be allowable if re-written in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for the indication of allowability as to such subject matter. With respect to the statements as to the reasons for allowability provided, Applicants concurs that the prior art of record does not show or suggest the elements of the claims recited as set forth in the Office Action. In addition, Applicants note that the claims also recite other elements that are not shown or suggested by the art of record. Applicants assert that the present claims are allowable for at least the reason that the art of record does not show or suggest all of the recited elements of the claims. Thus, Applicants assert that each claim is allowable in view of the complete language recited therein, as well as, equivalents. Applicants respectfully assert that the scope of each of claim as allowed is to be determined from the actual claim language including all equivalents.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding this response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,



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